In re Patent Application of:
DEQUINA ET AL
Serial No. **10/725,764**
Filed: **DECEMBER 2, 2003**

REMARKS

An editorial correction has been effected in the specification and claims 12-19 have been replaced by new claims 20-27. Reconsideration of this application in light of the foregoing amendments and following remarks is respectfully requested.

The outstanding office action raises three issues regarding previously submitted claims 12-19. The first issue is the objection to the claims based on a number of informalities as specifically delineated on pages 2-5 of the outstanding office action, many of which allege a lack of antecedent basis and question the use of the terms "low" and "high".

The second issue is the rejection of claims 12-16 under the second paragraph of 35 U.S.C. 112, regarding a specifically identified phrase in claim 12.

The third issue is the allegation that claims 12-19 are anticipated by the patent to Berg et al, 6,107,844.

As will be demonstrated below, applicants respectfully submit that replacement claims 20-27 obviate each objection and ground of rejection raised in the outstanding office action, whereby the application is in condition for allowance.

More particularly, claims 20-27 contain apparatus claim 20, upon which claims 21-24 depend, and method claim 25, upon which claims 26 and 27 depend. The phraseology of replacement claims 20-27 has been chosen in light of the specific objections and grounds of rejection raised in the outstanding office action, and is believed to concisely define applicants' invention in a manner

which is both clear and concise and which is not disclosed by the prior art cited in the outstanding office action.

For example, in claim 20, which replaces claim 12, the phase node voltage is initially characterized in a phrase that recites that the PHASE node condition threshold detector is operative to monitor a phase node voltage at a PHASE node or common node between the UFET and LFET. Similarly, step (a) of claim 25 recites monitoring and LGATE voltage, a UGATE voltage and a phase node voltage.

Further, claim 20 simply recites "type" of switching FET, rather than "the" type….

Moreover, in place of the phrase "the phase node voltage to go high", claim 20 recites that the switching control operator is operative to trigger turn-on of said UFET, which causes the phase node voltage to increase from a first voltage level to a second voltage level higher than said first voltage level. This phraseology is believed to answer the inquiry and clarify the objection in the second paragraph on page 3 of the office action.

With respect to the third objection on page three, as pointed out above, the initial portion of the claim recites that the PHASE node condition threshold detector is operative to monitor a phase node voltage, so that subsequent recitation of "said" phase node voltage has antecedent basis. The same is true for the fourth objection at the top of page 3 of the outstanding office action.

With regard to the initial objection of claim 13, the phrase "the absence" is not found in any of replacement claims, 20-27.

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The second objection directed against claim 13 is believed to have been obviated by the language of the replacement claims, which do not recite either "high" or "low", but recite the phase node having reached "a prescribed negative polarity voltage threshold" or having reached "a prescribed positive polarity voltage threshold".

With respect to the objection to claim 13 at the bottom of page 3 of outstanding office action, the limitation referred to is found in previously submitted claim 14, not claim 13. The same is true of the objection in the first paragraph on page 4 of the outstanding office action.

The replacement claims are believed to be clear by the use of the phrase "following a predetermined blanking delay subsequent to…."

The objections directed against claims 14 and 15, as well as claims 17, 18 and 19, on pages 4 and 5 are believed to be obviated by the language referenced above, as the specific objections directed to claims 18 and 19 are effectively those directed against claims 12 and 13, addressed previously.

Withdrawal of the objections to the claims is, accordingly, earnestly solicited.

With regard to the second issue, specifically, the rejection of claims 12-16 under the second paragraph of 35 U.S.C. 112, the following comments are offered.

As pointed out above, claims 20-24, which replace claims 12-16, do not contain the phrase "the phase node voltage to go high." Instead, claims 20-24 recite that triggering turn-on of

the UFET causes the phase node voltage to increase from a first voltage level to a second voltage level higher than said first voltage level. Thus, there is a reference voltage, namely the first voltage level, relative to which the comparison recited in the claim is made. Withdrawal of the rejection of claims 12-16, is, therefore, respectfully requested.

The remaining, or third, issue raised in the outstanding office action is the allegation that claims 12-19 are anticipated by the patent to Berg et al, 6,107,844: As pointed out above, this rejection is respectfully traversed.

More particularly, by clarifying the language of the replacement claims to obviate the objection and rejection under 35 U.S.C. 112, discussed above, applicants respectfully submit that it is clear that the claims distinguish over the patent to Berg et al by reciting the operations that are represented by the timing diagrams of Figures 4 and 5.

Specifically, Figure 4 shows three successive cases I, II and III in Figures 4C, 4D and 4E, respectively, that may be involved in the subsequent turn-on of the UFET following a prescribed blanking delay and respectively different prescribed conditions, following the turn-off of the LFET, shown at 411.

As recited in claim 20, and as shown at case I in Figure 4C, two things are required to control the turn-on off the UFET subsequent to the turn-off of the LFET. The first is a blanking delay shown at 420-D, which is subsequent to the turn-off of the LFET. The second is the phase node voltage shown at 420 reaching a prescribed negative polarity, shown at 421, following the blanking delay subsequent to turn-off of the LFET. This is clearly recited in claim 20, referenced above.

Claim 21 addresses case II wherein the phase node voltage is increased from a first voltage level at 430 to a prescribed positive polarity voltage threshold, shown at 431. This is clearly recited in claim 21, which recites:

> "in response to said phase node voltage having increased from said first voltage level to said prescribed positive polarity voltage threshold."

The third case III corresponds to the case that a prescribed time-out occurs without either of the prescribed positive and negative polarity voltage thresholds having been reached. This is shown in Figure 4E, wherein a delay 440-TD occurs and then the UFET is turned on at 441. This is clearly recited in claim 22.

Claims 23 and 24 delineate the situation shown in Figures 5A-5C, which detail the controlled turn-off of the UFET and the subsequence turn-on of LFET. Turn-off of the UFET is initiated by the high-to-low transition 501 of the PWM waveform of Figure 5A as described in paragraph [028] on page 13 of the specification. Thereafter, the PHASE node and UGATE node are monitored for prescribed switching operations of the LFET.

To this end, claim 23 recites that the switching control operator is operative, in response to turn-off of the UFET, and in response to a UGATE voltage and the UGATE dropping to a voltage level that is a prescribed value above the phase node voltage, shown at 531 in Figure 5C, to trigger a prescribed time-out (the 10 nanosecond delay) and then turn-on the LFET in response to expiration of the prescribed time-out.

Claim 24 claims the situation in Figure 5D, wherein the switching control operator is operative, in response to turn-off

of the UFET, and in response to the phase node voltage reaching a predetermined threshold voltage, shown at 511, to turn-on the LFET.

Independent claim 25, upon which claims 26 and 27 depend, includes step (a), which, as pointed out above, recites monitoring of the LGATE voltage, the UGATE voltage and the phase node voltage.

Step (b) of claim 25 specifies that, in response to turn-off of the LFET, and in response to the phase node voltage at the PHASE node having reached a prescribed negative polarity voltage threshold, following a predetermined blanking delay subsequent to turn-off of the LFET, triggering turn-on of the UFET, thereby causing the phase node voltage to increase from a first voltage level to a second voltage level higher than said voltage level. As pointed out above, this is clearly shown in Figure 4C, which shows the blanking delay 420-D and the phase node voltage reaching a negative polarity 421, so that the phase node voltage increases as shown at 422. Recitations similar to those in claims 21 and 22 are found in claims 26 and 27.

The patent to Berg et al, 6, 107,844, shows, for example, in Figures 2 and 6, waveform diagrams associated with the turn-on and turn-off of the MOSFETs M1 and M2 in Figures 1 and 5, respectively. The timing diagrams also show delineated timing marks to identify specific portions of the waveforms.

Also, the patentees define what is known as dead-time, which is a time interval when both MOSFETs M1 and M2 are off and not conducting current. This is shown, for example, in the timing diagram of Figure 2 as interval t1-t2.

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Applicants do not dispute what the patent to Berg et al actually shows. However, what applicants do dispute is the allegation that the claims are anticipated by the patent.

More particularly, the explanation of the rejection in the third paragraph, on page 6, of the outstanding office action is "generalized", to the extent that the claims have been examined from a "generalized" standpoint. However, the replacement claims more particularly delineate specific threshold conditions and blanking delays that precede the threshold conditions, which are monitored and used to control the switching of the UFET and LFET, in accordance with the present invention, as discussed at length above. The patent to Berg et al is silent with respect to the particular conditions that are monitored as claimed, to trigger turn-on of the UFET and turn-on of the LFET, subsequent to turn-off of the LFET and turn-off of the UFET, respectively. It is respectfully submitted that upon reconsideration it will be recognized that replacement claims 20-27, by concisely delineating the operations of the present invention shown in the timing diagrams of Figures 4A-4E and 5A-5D, which are not addressed by Berg et al, render the present application in condition for allowance.

Favorable reconsideration and a Notice of Allowability of claims 20-27 is, accordingly, earnestly solicited.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number **703-872-9306** to the COMMISSIONER FOR PATENTS, this 24 day of January 2005.

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